A Comparative Study of Different 7T SRAM Cells Enhancing the Throughput for Low Power Operations

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This paper presents a comprehensive comparative analysis of three 7T SRAM cell designs at the 32nm technology node with a supply voltage of 1.2V, evaluating Static Noise Margins, Write Time, Current Ratio, and Power Consumption through SPICE simulations. While sharing a common memory core, the designs feature distinct port configurations that significantly impact performance. The single-port, single-ended 7T-1 demonstrates superior HSNM (436 mV) and read power efficiency, while the Schmitt trigger-based 7T-3 achieves the highest write margin (599 mV), lowest write/hold power, and fastest write operation (0.1 ns critical write time). All designs show similar current ratios, with 7T-1 and 7T-3 exhibiting approximately double the ratio of 7T-2. Our analysis reveals fundamental trade-offs: 7T-2 offers the best overall stability balance, 7T-1 excels in power-sensitive applications despite modest write margin reduction, and 7T-3 provides exceptional write performance at the cost of read/hold stability. These findings provide critical insights for SRAM design optimization in low-power applications, particularly for IoT and portable computing devices.

Keywords: SRAM, HSNM, RSNM, Dynamic power, static power, 7T

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1 Introduction

With the rise [1] of portable computing devices and IoT devices, the need for high processing speed and low-power processors has also increased. Processors utilize an internal cache to enhance operational speed, which consists of an array of SRAM cells. A majority of total SoC power consumption can be attributed to SRAMs [2], making power reduction in SRAM essential for designing lower-power IoT devices. SRAM power consumption is divided into dynamic and static components. As the charging and discharging of bitlines constitutes the major portion of dynamic power consumption [3], single-ended bit cells have become popular for power reduction. Another power reduction method involves lowering the supply voltage [4], though this reduces SNM and compromises data stability [5].

Cell layout area represents another critical metric, where increasing transistor count leads to greater cell area [6]. Even minor area increases can significantly expand cache size. While higher transistor counts are undesirable, conventional 6T cells demonstrate unreliable performance at smaller technology nodes, making 7T cells the current standard [7].

This work simulates and compares three 7T SRAM cells (shown in Fig. 1) at 1.2V supply voltage using SPICE software at the 32nm technology node. The study evaluates these designs across stability, operation speed, and power consumption metrics. The paper is organized into five sections: Section 1 introduces the topic, Section 2 reviews existing 7T cell topologies, Section 3 explains the operation of the test cells, Section 4 presents and compares simulation results, and Section 5 provides conclusions.

2 Literature Review

This section reviews various 7T SRAM topologies, most sharing a common memory core of two cross-coupled inverters with an access transistor controlling feedback via the W1 signal.

Mehrabi et al. [8] proposed a single-ended dual-port configuration with separate read/write ports, enabling optimal access transistor sizing for improved stability. Their virtual ground technique reduces leakage power during standby by disconnecting the cell from actual ground and connecting to a virtual ground node. A transistor switch controls this node, remaining off during idle periods to raise ground potential and suppress pull-down network leakage current, minimizing static power dissipation. During active operations, the switch reconnects virtual to actual ground. However, this approach increases write delay and risks data degradation under extreme voltage/temperature variations.

The 7T-3 cell [9], designed for IoT applications, prioritizes low power consumption and high stability in energy-constrained environments. Its Schmitt trigger mechanism improves noise immunity and mitigates process variations, ensuring reliable operation under dynamic IoT conditions. The single-ended configuration reduces bitline switching activity, further lowering dynamic power. While the Schmitt trigger enhances read/write stability, it introduces design complexity that can increase write delay, and the single-ended architecture may compromise read speed versus differential designs, illustrating the stability-performance trade-offs in resource-constrained applications.

The 7T-1 cell [10] features a single-port, single-ended design with an isolated read port that separates the read path from the memory core, improving read stability. Optimized for subthreshold operation, it maintains stability down to 180mV, with the single-ended configuration providing

enhanced noise resilience.

Oh et al. [1] proposed a differential read/write cell featuring an inverter feedback loop with a stacked inverter memory core lacking an access transistor for feedback control. The differential port and stacked inverter architecture result in higher power consumption and reduced ON current.

The 7T-2 cell [11] implements a single-ended dual-port design that is RSNM-free, isolating the read path from the memory core to prevent read operations from affecting data integrity. This dual-port architecture effectively eliminates read-write conflicts.

3 Overview of 7T SRAM Architectures and Their Operation

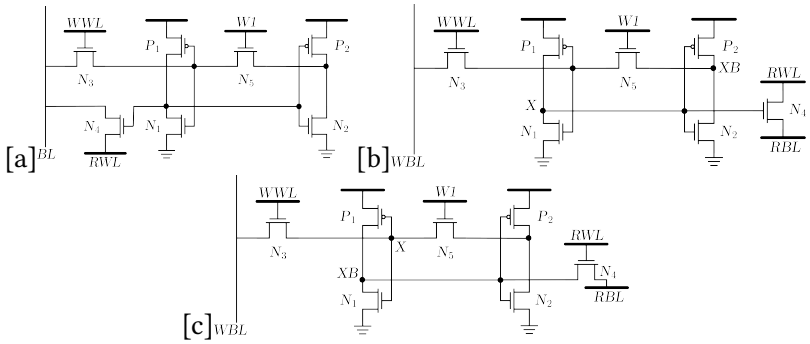


Figure 1: (a) 7T-1 (b) 7T-2 (c) 7T-3

In the 7T-1 design [10], the bitline is precharged and the RWL is pulled to ground level during read operations. If the stored data is logic '1', the read access transistor activates and discharges the bitline through the read path; if the data is logic '0', the bitline remains charged. During hold operations, WWL is set to '0' and RWL to '1', deactivating both access transistors. To optimize write performance, the feedback between cross-coupled inverters is weakened by deactivating the feedback control transistor (W1 set to '0'). Data is written by placing its inverse on the bitlines while setting WWL to '1'.

The 7T-2 design [11] operates identically to 7T-1 during write and hold modes. For read operations, RBL is grounded while RWL remains at '1' (its state for all operations). Similar to 7T-1, when the stored data at node X is '1', the read access transistor activates, allowing current flow through the read path.

The 7T-3 design [9] differs significantly in write operations, where the bitlines carry the same data as what needs to be stored. For reading, RWL is set to '1' and RBL is precharged. If the stored data is '1' (with XB at '0'), RBL discharges; otherwise, it remains charged. A key distinction is that the storage node XB lies in the discharge path during read operations.

Table 1 summarizes these control signals for different operations. Key terms include: 'PC' for Precharged, 'DATA' for the desired stored value, 'DATAB' for its logical inverse, and 'N/A' for signals not applicable to the design.

Table 1: Signals for Hold, Read, Write operation of 7T-1, 7T-2, 7T-3 cells.

2*Signal	Hold			Read			Write		
	7T-1	7T-2	7T-3	7T-1	7T-2	7T-3	7T-1	7T-2	7T-3
RWL	1	1	0	0	1	1	1	1	0
WWL	0	0	0	0	0	0	1	1	1
W1	1	1	1	1	1	1	0	0	0
WBL	N/A	PC	PC	N/A	PC	PC	N/A	DATAB	DATA
RBL	N/A	PC	PC	N/A	0	PC	N/A	PC	PC
BL	PC	N/A	N/A	PC	N/A	N/A	DATAB	N/A	N/A

4 Results and Comparison

4.1 Static Noise Margin Analysis

Static noise margin (SNM) is the most effective metric for quantifying bit cell reliability during hold, read, and write operations [12]. The comparison of SNM for the three designs is shown in Fig. 2. Both 7T-1 and 7T-2 feature isolated read paths, making them read SNM-free - their read SNM equals their hold SNM.

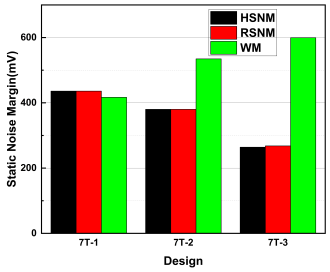


Figure 2: Static noise margins of 7T-1, 7T-2, 7T-3)

Rather than using traditional write SNM calculated from the largest square in the butterfly curve, we employ write margin. This metric better quantifies cell resilience during write operations [9]. The required data is placed on the bitline while the WWL signal varies from GND (0V) to VDD (1.2V). Write margin is defined as the difference between WWL and VDD at the moment when X and Xb flip [13]. For ease of analysis , we have tabulated the hold, read and write margins in Table 2.

Table 2: Hold and Read SNM ,and Write margin values for 7T-1, 7T-2, 7T-3)

Design	Hold (mV)	Read (mV)	Write (mV)
7T-1	436	436	417
7T-2	380	380	534.66
7T-3	264	268	599.56

Regarding stability across operations, the 7T-1 design maintains consistent hold and read margins of 436 mV, though with a relatively lower write margin of 417 mV. The 7T-2 design achieves

a strong balance, showing 380 mV for both hold and read stability along with a substantial write margin of 534.66 mV. In contrast, 7T-3 demonstrates the lowest hold (264 mV) and read (268 mV) margins but compensates with the highest write margin (599.56 mV). This superior balance in 7T-2 stems from its isolated read port (separated from the storage node) and dedicated read/write ports, which enhance stability for both operation types.

4.2 Power Consumption

As the scale of technology nodes is miniaturized and battery life becomes a major design concern, power consumption becomes a crucial parameter [14]. Power consumption of SRAM can be divided into two components: dynamic and static. Dynamic power is the power consumed by the memory circuit in read and write operations. Static power is caused by leakage currents during the hold operation [15], which is especially significant in nanoscale technologies due to increased leakage current.

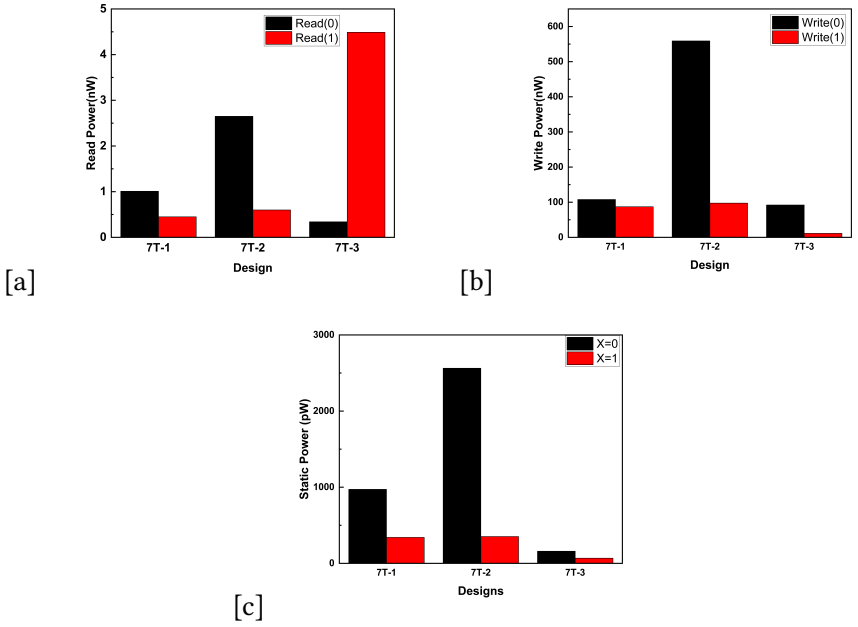


Figure 3: (a) Read Power consumption (b) Write Power (c) Static Power consumption of 7T-1, 7T-2 and 7T-3

Fig. 3(a)-(b) shows the values of read and write power for logic '1' and logic '0' bit values for the three designs. During read operations, 7T-2 consumes the highest power at 2.65 nW for reading '0' and 0.6 nW for reading '1'. In comparison, 7T-1 records lower consumption at 1.01 nW and 0.45 nW, respectively, while 7T-3 is the most efficient for reading '0', consuming just 0.341 nW, though it uses 4.49 nW for reading '1'.

For write operations, 7T-2 again shows the highest power consumption at 558.99 nW for writing '0' and 97.51 nW for writing '1'. 7T-1 consumes 107.67 nW and 87.05 nW for the same opera-

tions, while 7T-3 is the most efficient for writing '1', consuming only 11.4 nW.

Static power consumption results, shown in Fig. 3(c), further highlight the superior efficiency of 7T-3. For a logic state of '0', it consumes just 159.42 pW, much lower than 971.96 pW for 7T-1 and 2562.7 pW for 7T-2. In the logic state of '1', 7T-3 consumes only 68.05 pW, compared to 340.9 pW and 351.97 pW for 7T-1 and 7T-2, respectively.

Overall, while 7T-2 and 7T-1 consume more power, particularly in write and static operations, 7T-3 demonstrates superior power efficiency across most scenarios, making it ideal for applications prioritizing low power consumption.

4.3 Ion/Ioff

The I_{on}/I_{off} current ratio, representing the relationship between read and leakage currents, serves as a critical parameter in SRAM design [16]. A higher current ratio enables greater integration density of bit cells per column through optimized sense amplifier sharing, thereby simplifying the read peripheral circuitry. This makes SRAM cells with elevated I_{on}/I_{off} ratios particularly advantageous for memory architecture optimization.

As shown in Fig. 4(a), all three evaluated designs demonstrate comparable current ratios, with 7T-1 and 7T-3 exhibiting the highest values - approximately double that of 7T-2. This significant difference in current ratio suggests superior performance characteristics for 7T-1 and 7T-3 in terms of read current efficiency relative to leakage.

4.4 Dynamic Write Analysis

In SRAM bit cell design, static write margin (WM) analysis typically assumes an infinite pulse width for theoretical evaluation. However, practical write operations depend on finite pulse durations, making it crucial to determine the minimum wordline (WWL) pulse width required for successful write operations - known as the critical write pulse width (T_{crit}). This study evaluates T_{crit} using the methodology outlined in [12]. When the applied WWL pulse width falls below T_{crit} , write failures become probable, necessitating operational WWL pulses that always exceed this critical duration to ensure reliable memory operation.

As shown in Fig. 4(c), the critical write times for the three test cells demonstrate significant variation. Both 7T-1 and 7T-2 require T_{crit} values of 5 ns, while 7T-3 achieves successful writes with a substantially shorter T_{crit} of only 0.1 ns. This remarkable difference shows that 7T-3 outperforms the other cells by two orders of magnitude in this critical performance metric, making it particularly suitable for high-speed applications.

4.5 Comparison

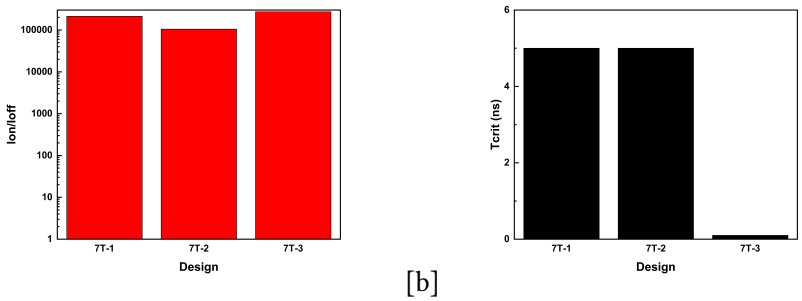
In the 7T-1 design, the read and write operations share a common bitline, whereas 7T-2 and 7T-3 employ separate bitlines for read and write operations. The use of separate bitlines appears to significantly enhance write stability, as evidenced by the superior write margins of 7T-2 and 7T-3. However, the shared bitline configuration of 7T-1 demonstrates a clear advantage in dynamic power efficiency compared to the separate bitline designs.

The second key design difference lies in the read port architecture. Both 7T-1 and 7T-2 feature an RSNM-free (Read Static Noise Margin-free) read port, which contributes to their improved

read and hold stability relative to 7T-3. This stability, however, comes at the cost of higher static power consumption in both 7T-1 and 7T-2 compared to 7T-3.

These observations highlight the inherent trade-off between stability and power consumption in SRAM design—optimizing one parameter often leads to degradation in the other. Consequently, a compromise must be struck based on application requirements. While 7T-2 achieves the best overall stability, 7T-1 emerges as the superior choice for power-sensitive applications, offering significantly reduced power consumption at the expense of a modest reduction in write margin.

Under temperature variations, 7T-2's power consumption would likely increase further, and 7T-3's already-low read/hold stability would degrade. Thus, 7T-1 emerges as the most temperature-tolerant design. At advanced nodes like 32 nm, process variations—which cause threshold voltage fluctuations—introduce additional uncertainty. While exact impacts are hard to predict, 7T-1's consistently low power consumption across operations suggests it will maintain better average efficiency under such variations.



[a] [b]

Figure 4: (a) Current Ratio (b) Critical Pulse width for write operation of 7T-1, 7T-2 and 7T-3

From Fig.4(b) it is evident that 7T-3 shows the minimum critical time pulse width of only 0.1ns, while both design 7T-1 and 7T-2 need 5ns for data to be stored.

5 Conclusion

In this paper, three 7T SRAM cells with the same memory core—consisting of an inverter pair in feedback with an access transistor controlling the feedback—are analyzed. The cells vary in their implementation of read and write ports, and their stability shows a high dependence on these configurations.

In terms of HSNM and RSNM, the isolated read-port designs, 7T-1 and 7T-2, achieve the highest values of 436 mV and 380 mV, respectively. However, the 7T-3 cell excels in write margin with 599.56 mV, attributable to its Schmitt trigger-based design. The write margin of 7T-2 follows closely at 534.66 mV, while 7T-1 trails at 417 mV, making 7T-2 the most balanced in overall stability.

Power consumption during read operations is lowest in 7T-1, whereas 7T-3 outperforms in write and hold power efficiency. All three designs exhibit similarly high current ratios. Notably, 7T-3 achieves the shortest write time (0.1 ns), far surpassing the 5 ns required by 7T-1 and 7T-2.

The analysis reveals a clear trade-off between performance metrics: 7T-1 offers high read/hold stability and low power but suffers in write margin and speed; 7T-2 balances decent read margin and high write margin yet consumes more power and has slower write times; 7T-3 boasts superior write margin and speed but lags in read/hold SNM.

Further analysis of different port configurations' ability to withstand temperature and process variations could help confirm the earlier speculations. Additionally, comparing port designs in higher transistor-count cells may reveal new limitations not apparent in 7T cells. Testing these designs' performance for near- or sub-threshold operation would be valuable for ultra-low-power applications.

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