# A Fully-Differential-Double-Folded-Cascode-Push-Pull OTA with 151 dB CMRR

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A fully-differential-double-folded-cascode-push-pull(FDDFCPP) OTA is presented. The OTA is optimized for large values of the power-supply-rejection-ratio(PSRR) and common-mode-rejection-ratio(CMRR). The FDDFCPP OTA consists of a fully-differential-folded cascode as the first stage, which provides a large signal swing and high DC gain. The 2nd stage of the proposed OTA is a push-pull amplifier stage, which improves the transient behavior of the proposed OTA. The proposed circuit is frequency compensated using Miller compensation. The proposed design is simulated using an Electric-VLSI tool with an LTspice simulator using 180nm CMOS technology. The proposed OTA provides a CMRR of 151.4dB(DC), PSRR of 52.40dB(DC), unity-gain-frequency(UGF) of 37.15MHz with DC gain of 32.5dB, phase-margin of 56.57() and power consumption of 0.52mW with capacitive load of 3pF.

**Keywords:** Folded-cascode, Push-pull, CMRR, PSRR.

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# 1 Introduction

Analog and mixed-signal integrated circuits have an operational transconductance amplifier as the main fundamental building block. One of the common architectures utilized in OTA to achieve a large DC gain and a large signal swing is the folded cascode (FC) amplifier, either as a single stage or as the first stage of a multi-stage amplifier. The PMOS input FC-OTA is preferred over its NMOS counterpart due to its low flicker noise, higher non-dominant poles, and lower input common mode level. Over the years, different architectures of FC-OTA have been developed, which ultimately result in enhanced values of DC gain, Gain-bandwidth-product(GBW), slew-rate, and lower static power dissipation. The recycling folded cascode(RFC) OTA architecture proposed in [1] utilizes current mirror MOSFETs, which are used as driving transistors rather than the folding node for small-signal current generated by input differential driving transistors, as is the case with conventional FC-OTA. Authors in [1] proposed reusing previously idle devices within the signal path to perform additional tasks, leading to improved characteristics without increasing area or power consumption. The proposed design achieves twice the $G_m$ as compared to conventional FC-OTA. There is an improvement of around 8–10 dB in DC gain, and the slew-rate(SR) of RFC-OTA becomes three times that of FC-OTA, and the GBW of RFC-OTA becomes two times that of conventional FC-OTA.

In reference [2], the authors proposed an enhanced single-stage FC-OTA designed to efficiently drive large capacitive loads. The novelty of the proposed architecture lies in using adaptive biasing for both the input differential pair and the current folding stage. This approach ensures class AB operation, which results in large dynamic currents that are not limited by the quiescent currents, thereby achieving low static power consumption while maintaining high dynamic performance. In [2], adaptive biasing circuits are implemented using Flipped-voltage-followers(FVF) and quasi-floating gates(QFG) transistors, which results in a simple and compact design not requiring extra supply voltage. The presented solution reports performance enhancements in terms of SR. The class AB version achieves a 30.6 times higher SR compared to a conventional class A version using the same supply and bias currents. This enables OTA to handle large capacitive loads and rapidly changing output signals more effectively.

The research article in [3] presented a novel superclass—AB RFC OTA designed to enhance metrics such as SR and GBW while maintaining power efficiency, particularly for low-voltage and low-power applications. The design combines the benefit of the recycling folded cascode(RFC) OTA with adaptive biasing and local-common-mode-feedback (LCMB) techniques. The core of the proposed architecture utilizes an adaptive bias circuit in place of a constant current source that biases the differential pair. This allows for very low static currents while enabling large dynamic currents for significant input signals, thus improving SR without being limited by quiescent current. The adaptive biasing is implemented by FVFs.

The authors of [3] integrate LCMFB at the load of the differential pair, further enhancing performance parameters and current efficiency. The proposed novel architecture provides improved and enhanced values for SR and GBW.

The research article in [4] presented an enhanced architecture with the objective of increasing the performance of the conventional RFC op-amps, particularly in terms of DC gain and GBW, while enhancing other critical parameters such as noise, settling time, and distortion. The high-RFC is an improvement over the conventional RFC, with improvement achieved by shortening two nodes within the RFC circuit. This modification is designed to amplify the transconductance at the output, which directly leads to high DC gain and large GBW. In the research article [5], a Local-positive-feedback(LPFB) technique is presented, which provides enhancement over conventional FC-OTA in terms of important specifications. The proposed enhanced FC-OTA has a higher GBW and slew-rate. The implementation of the proposed solution involves reusing the current generated by the input transistors through the proposed local-positive-feedback(LPFB) loop to provide additional transconductance and negative resistance. In this study, to overcome the low efficiency of conventional FC-OTA, the authors proposed a PMOS-input enhanced FC-OTA by using an LPFB loop. The loop is achieved by reusing the current generated by the input transistors by the use of a transconductance circuit to drive idle folded transistors, which results in an increase in effective transconductance of the input stage, with the use of a LPFB loop a negative resistance introduced at the input stage which improves DC gain, LPFB loop allows large dynamic current not limited quiescent currents hence enhances SR. In reference [6] authors identify FVF as a fundamental cell for low-power and low-voltage analog circuit design. The authors provide a comprehensive overview, including a detailed classification of its basic topologies. A research article mentions that the FVF cell operates effectively at very low supply voltages, making it suitable for modern CMOS processes where supply voltages are continuously decreasing. The FVF cell is capable of class AB operation, which allows it to deliver large peak currents while maintaining low quiescent power consumption. FVF also exhibits very low impedance at its output node, which enables it to source large currents, improving transient performance.

The research article in reference[7] presents a novel design technique for low-voltage, power-efficient superclass AB CMOS-OTA. The major novelty of the proposed work lies in combining class AB differential input stages with local-common-mode-feedback (LCMFB). The proposed method aims to overcome the limitations of the conventional class A OTA, which faces a trade-off between slew-rate and static power consumption. It also addresses issues with previous class-AB amplifiers that often degrade the small signal performance or require complex additional circuitry. LCMFB provides dynamic current boosting, enhanced GBW, and near-optimal current efficiency without sacrificing static power consumption. The proposed design ensures that the large dynamic currents are generated directly in the output branches, eliminating the need for internal replication and improving current efficiency. In the research article of reference[8], the authors detail the conversion of a low-voltage, low-transistor-count, and wide-swing multistage pseudo-class-AB amplifier into a true class-AB amplifier. The primary motivation of this conversion is to address the power consumption inefficiencies of the pseudo-class-AB design, which suffers from a load-dependent bias current. The pseudo class-AB amplifier has a significant drawback, as mentioned in the article, of total bias current increases proportionally with the output sinking current due to a current mirror in the output stage. This characteristic leads to reduced efficiency. The authors propose a conversion to a true class-AB amplifier by employing gate-drain feedback which combines two-inverting common-source amplifiers into a single-stage non-inverting stage; This modification leads to a bias current profile independent of load current. The design utilizes reverse-nested Miller compensation(RNMC) to achieve stability across a wide range of capacitive and resistive loads. The advantages of this useful conversion are the enhancement of the value of UGW and slew-rate, and reduction in the value of the compensation capacitor. Reference[9] details the design and simulation of a fully-differential opamp intended for high-speed 12-bit pipeline ADC applications. The opamp incorporates double-folded cascode architecture with a class-AB output stage and continuous-time CMFB network. The proposed design aims to improve efficiency and reduce power dissipation, especially by minimizing slew-limiting in the first stage. The CMFB network is crucial for controlling common-mode voltages at various nodes and enhancing the CMRR of the opamp. It also helps in preventing common-mode components from saturating across different stages. A high-swing bias network is employed to minimize errors and scale the current effectively. The proposed opamp operates from a 1.8 supply, provides a DC gain of 117 dB, a phase-margin of 65 degrees and a CMRR of 72 dB. Its settling time is sufficient for driving the pipeline ADC. The authors in reference[10] propose a novel folded-cascode opamp that utilizes a nested gain-boosting technique to achieve high gain and high speed, making it suitable for high-speed and high-resolution pipelined ADC. The gain-booster proposed opamp in [10] incorporates a nested gain-boosting technique where the gain-booster in the signal path consists of a two-level recursive folded cascode amplifier. This approach is designed to enhance gain without significantly degrading overall BW. The presented design aims for an excellent trade-off between high DC gain at a high sampling rate and avoiding slow settling components, which is crucial for high-speed and high-resolution applications. The core amplifier uses a p-type input differential pair folded-cascode structure with low input capacitance; the gain-boosting amplifiers are designed with a stringent unity gain frequency requirement. A dual-phase switched capacitor common mode feedback(SC-CMFB) is applied to the core amplifier for a large output swing, while continuous time(CT)-CMFB is used in the gain-boosting amplifier. The proposed solution of [10] is able to achieve large values of DC gain, high speed, bandwidth(BW), and fast settling, critical for pipelined ADC applications. The research paper in reference[11] presents a novel cross-coupled cascode feedback technique for the design of a two-stage OTA, design also incorporates push-pull output stage for driving large capacitive load, the proposed design resulted in enhancement of SR and UGF. The proposed solution also achieves large values of CMRR and PSRR at high frequency for a large capacitive load of 400pF, but at the cost of power dissipation of 3.17mW and phase-margin of 48.50().

## 2 Proposed OTA design

The proposed p-type FDDFCPP OTA consists of two stages, with the first one being a folded-cascode stage, which is fully differential, and a push-pull amplifier as the second stage. The circuit implementation of the FDDFCPP OTA employs $M_1$ and $M_2$ as the main driving transistors of the input differential pair, $M_4$ and $M_5$ acting as NMOS loads, which also act as folding nodes for a small signal current. The double folded-cascode stages are implemented through transistors $M_6$-$M_{17}$ with opposite polarity outputs of differential pairs connected to the source node of transistors $M_6$-$M_7$ and $M_{12}$-$M_{13}$. Transistors $M_8$-$M_{11}$ and $M_{14}$-$M_{17}$ form the cascode pair for two sides of the proposed OTA. Push-pull 2nd stage is implemented with transistors $M_{18}$-$M_{21}$. A resistor-averaged CMFB network is being utilized in the design of the proposed OTA to provide balanced swing at the output node and to improve rejection of common-mode disturbances, which results in improvement of CMRR. The novelty of the proposed design lies in the overall architecture of the design, where a double-folded configuration is implemented through a common gate stage with a cascode current mirror, and the 2nd stage is implemented as a push-pull output stage rather than the conventional class-A or widely adopted class-AB stage. The common gate stage helps to achieve wide-bandwidth operation for the proposed OTA, as it exhibits no Miller multiplication of capacitances. Push-pull stage drives a large current in the output capacitance, which improves the slew-rate performance of the presented architecture. The W/L aspect ratios of various transistors employed in the design of the proposed OTA are mentioned in Table 1. The proposed design makes use of various biases and supply voltages, which are given in Table 2.

Table 2: Bias voltages (volts) in proposed OTA

| Voltages | Values |
|---|---|
| $V_{DP1}$ | 0.65 |
| $V_{DP2}$ | 0.65 |
| $V_{CM}$ | 0.65 |
| $V_P$ | 0.4 |
| $V_N$ | 1.0 |
| VDD | 1.8 |

## 3 Circuit schematics and Gain calculations

Circuit schematics of the proposed OTA are given in Figure 1, and a small-signal circuit for the proposed OTA for DC gain calculation is shown in Figure 2. In this section, we derive the transfer function for the DC gain of the proposed OTA. In the small signal diagram, the first fully differential folded cascode stage is represented by a voltage-controlled current source in parallel with the respective stage conductances, and the 2nd stage is represented by the transfer function of the corresponding push-pull amplifier.

Table 1: Aspect ratio of MOSFETs used in proposed OTA.

| MOS NO. | W/L($\frac{\mu m}{\mu m}$) |
|---|---|
| $M_1$ | $\frac{0.8}{0.4}$ |
| $M_2$ | $\frac{0.8}{0.4}$ |
| $M_3$ | $\frac{1.6}{0.4}$ |
| $M_4$ | $\frac{0.4}{0.4}$ |
| $M_5$ | $\frac{0.4}{0.4}$ |
| $M_6$ | $\frac{0.4}{0.4}$ |
| $M_7$ | $\frac{0.4}{0.4}$ |
| $M_8$ | $\frac{0.8}{0.4}$ |
| $M_9$ | $\frac{0.8}{0.4}$ |
| $M_{10}$ | $\frac{0.8}{0.4}$ |
| $M_{11}$ | $\frac{0.8}{0.4}$ |
| $M_{12}$ | $\frac{0.4}{0.4}$ |
| $M_{13}$ | $\frac{0.4}{0.4}$ |
| $M_{14}$ | $\frac{0.8}{0.4}$ |
| $M_{15}$ | $\frac{0.8}{0.4}$ |
| $M_{16}$ | $\frac{0.8}{0.4}$ |
| $M_{17}$ | $\frac{0.8}{0.4}$ |
| $M_{18}$ | $\frac{6}{0.4}$ |
| $M_{19}$ | $\frac{12}{0.4}$ |
| $M_{20}$ | $\frac{6}{0.4}$ |
| $M_{21}$ | $\frac{12}{0.4}$ |
| $M_{22}$ | $\frac{1.6}{0.4}$ |
| $M_{23}$ | $\frac{0.8}{0.4}$ |
| $M_{24}$ | $\frac{0.8}{0.4}$ |
| $M_{25}$ | $\frac{0.4}{0.4}$ |
| $M_{26}$ | $\frac{0.4}{0.4}$ |

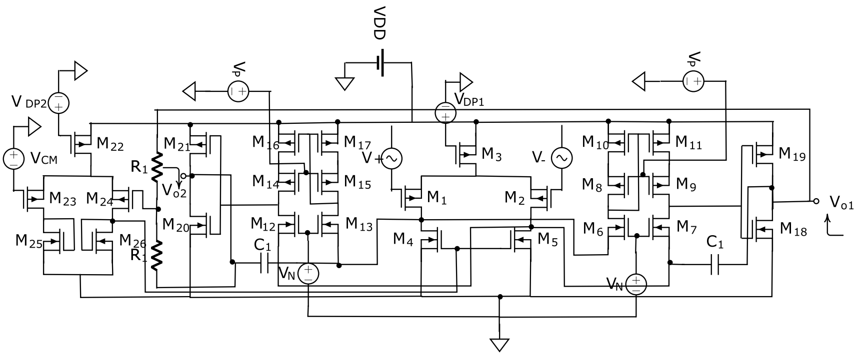


Figure 1: Circuit schematics of proposed OTA

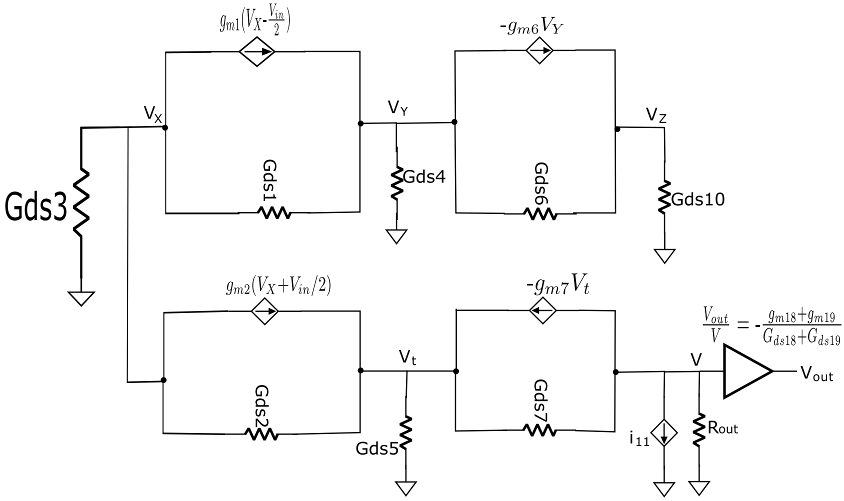


Figure 2: Small-signal circuit for the proposed OTA

$$\frac{V}{V_{in}} = \frac{k1k2}{(k1+k2)G_{ds9}}[G_{ds2} + \frac{g_{m1}g_{m11}}{g_{m10}}] \tag{2.1}$$

$$\frac{V_{out}}{V} = \frac{-(g_{m18}+g_{m19})}{G_{ds18}+G_{ds19}} \tag{2.2}$$

$$\frac{V_{out}}{V_{in}} = \frac{k1k2}{(k1+k2)G_{ds9}}[G_{ds2} + \frac{g_{m1}g_{m11}}{g_{m10}}](\frac{-(g_{m18}+g_{m19})}{G_{ds18}+G_{ds19}}) \tag{2.3}$$

$$k_1 = \frac{g_{m9}}{G_{ds2}+G_{ds7}} \tag{2.4}$$

$$k_2 = \frac{g_{m9}}{G_{ds7}} \tag{2.5}$$

Equation (1) represents the derived transfer function for DC gain of the fully differential double cascode first stage, equation (2) represents the DC gain of the push-pull stage, and the overall DC gain transfer function of the two stages of the proposed OTA is represented by equations (3, 4, and 5).

# 4 Simulations

Simulations results are obtained using Electric-vlsi tool with Lt-spice simulator using 180nm CMOS technology model file.

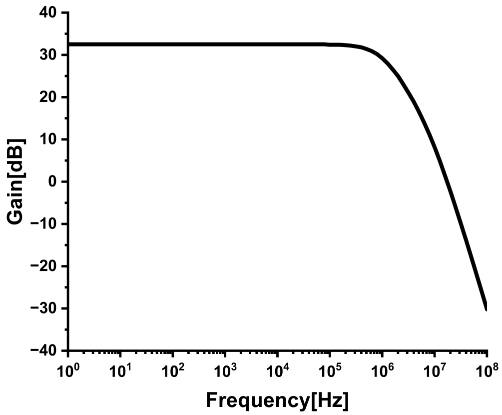


Figure 3: Gain-plot of proposed OTA

The Gain plot of the proposed FDDFCPP OTA is given in figure(3). The plot shows a DC gain value of around 32.5dB with unity-gain-frequency(UGF) of around 37MHz. The phase plot of proposed FDDFCPP OTA is shown in figure(4). The plot shows a phase-margin of around 57 (). The transient response to large step-input is given by the plot of figure(5). The positive and negative slew-rate(SR) obtain by simulation are 0.055(V/$\mu s$) and 0.8(V/$\mu s$) respectively. The simulated CMRR plot of proposed OTA against frequency is given in figure(6). The plot shows a DC value of CMRR of 151.4dB . The simulated plot of PSRR is given in Figure 7, the plot shows a DC PSRR value of 52.40dB.

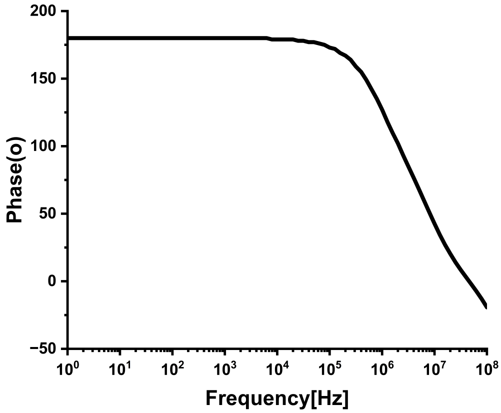


Figure 4: Phase-plot of the proposed OTA

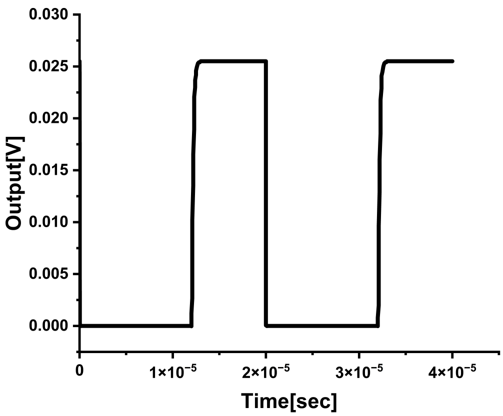


Figure 5: Transient response of proposed OTA

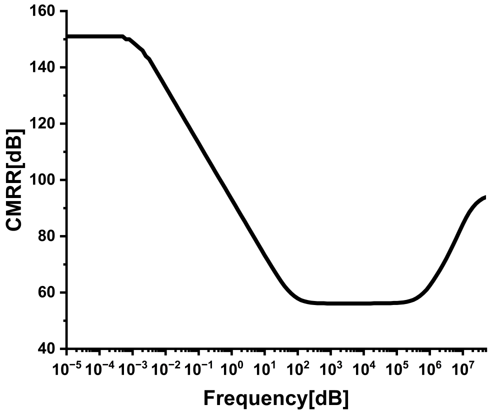


Figure 6: CMRR of proposed OTA

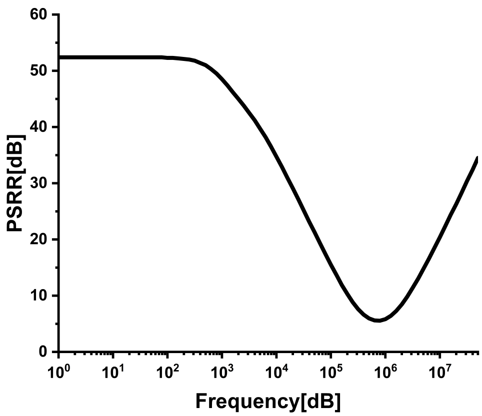


Figure 7: PSRR of proposed OTA

## 5 Conclusion

In this paper, a fully differential double-folded cascode Push-Pull OTA is presented. The proposed architecture consists of a fully differential folded cascode OTA with a push-pull 2nd stage. The design also employs a CMFB circuit. The proposed solution provides a very high value of CMRR of 151dB(DC). Because of the strong immunity of the proposed OTA to common-mode signals, it can be used in low-frequency biomedical circuits.

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